THOMSON COMPOSANTS MILITAIRES ET SPATIAUX

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Références TMS/7.289/88 FF

Saint-Égrève, le 7 Decembre 1988

OBJET : Notice TH7931D

Messieurs,

Veuillez touver ci-joint avec notre expedition, la notice du produit TH7931D dans sa version provisoire.

Cette notice est en cours d'impression et sera disponible d'ici quelques semaines, nous ne manquerons pas de vous en envoyer un exemplaire dès sa parution.

Comptant sur votre compréhension et restant à votre entière disposition pour tous renseignements,

Veuillez agréer, Messieurs, l'expression de nos salutations distinguées.

MN. GAUJOUR

THOMSON-CSF
TUBES ELECTRONIQUES

TH 7931 0

Drive Module*

for TH 7801A(Z), TH 7802A(Z), TH 7803A(Z), TH 7806, TH 7806(Z), TH 7831(Z) Linear CCD** Image Sensors

- **Provides the entire "image analysis" function***
- **Inputs:**
  — two external dc voltages
  — two external drive clocks
- **Five outputs:**
  — 50 Ω matched video signal with or without filtering
  — line synchronization signal
  — pixel synchronization signal
  — envelope signal for first 4 dark ref. pixels
  — external sample and hold pulses
- **Two adjustments possible (internally on board or by external signals)**
  — integration time
  — video signal readout time
- **105 mm × 65 mm PCB with HE 720 connector & female adaptor (total dimension: 115 mm × 75 mm)**

The TH 7931 drive module is designed to simplify the use of the TH 7801A , TH 7802A , TH 7803A , TH 7806, TH 7806(Z), TH 7831 linear CCD image sensors. (TH 7811 l'unico con controllo Ant.)

The board requires only two external dc voltages (+ 5 V and + 15 V) and provides all the necessary drive signals and dc biasing. In conjunction with the image sensor used, it delivers a low impedance video output signal, as well as "line" and "pixel" synchronization signals.

The integration time is adjustable to control the exposure and thus adapt to scene illumination. The signal readout time can also be adjusted as a function of the integration time and the operating mode chosen.
Integration and readout times can be adjusted on the board or by external drive clocks.

* Does not include optics or power supply.
** Charge Coupled Device.

Updates and replaces TEV 3636.

THOMSON-CSF / DIVISION TUBES ÉLECTRONIQUES
38 rue Vauthier / B.P. 305 / 92102 Boulogne-Billancourt Cedex / France / Tél. : (1) 46.04.81.75

DESCRIPTION

The TH 7931D comes as a 105 mm × 65 mm fitted printed circuit board. The schematic diagram is given in Figures 6 and 7.

An oscillator Z 5 (74HC4049) or an external clock with TTL output controls the readout output transfer phase Φ_T as well as the synchronization of the internal phase Φ_P with Φ_T. The frequency of the oscillator is four times that of the transfer clock Φ_T and twice the readout frequency of the video line output. The frequency division is ensured by bistables Z 8 and Z 10 (74HC74).

The integration time is defined by the rising edges from monostable Z 6 (74HC123) or an external TTL signal.

The video output signal is filtered by a low-pass filter (cut-off frequency F_{co} = 1 MHz), which eliminates switching noises introduced by the sensor's on- chip sampling circuit.

POWER SUPPLIES

Only two external power supplies are required :
- + 5 V / 30 mA connected to pin no. 1,
- + 15 V / 130 mA connected to pin no. 5

Pin no. 6 : is connected to the logic ground.
Pin no. 7 : is connected to the analog ground.

INPUT SIGNALS

They comprise two external clocks :
- Pin no. 11 : integration time command clock.
- Pin no. 10 : readout time command clock.

OUTPUT SIGNALS

The output signals are provided on :

- Pin no. 3 : composite video signal, measured on impedance load Z_L = 50 Ω, with max. ac level of 3 V peak-to-peak, superimposed on a dark reference dc level of 3 V (see figure 3) ; output impedance = 50 Ω.
- Pin no. 2 : line sync. signal
- Pin no. 8 : pixel sync. signal

  } TTL logic (see figure 2)
- Pin no. 4 : envelope signal of first 4 dark reference pixels in the line.
- Pin no. 9 : external sample-and-hold signal (see figure 2).

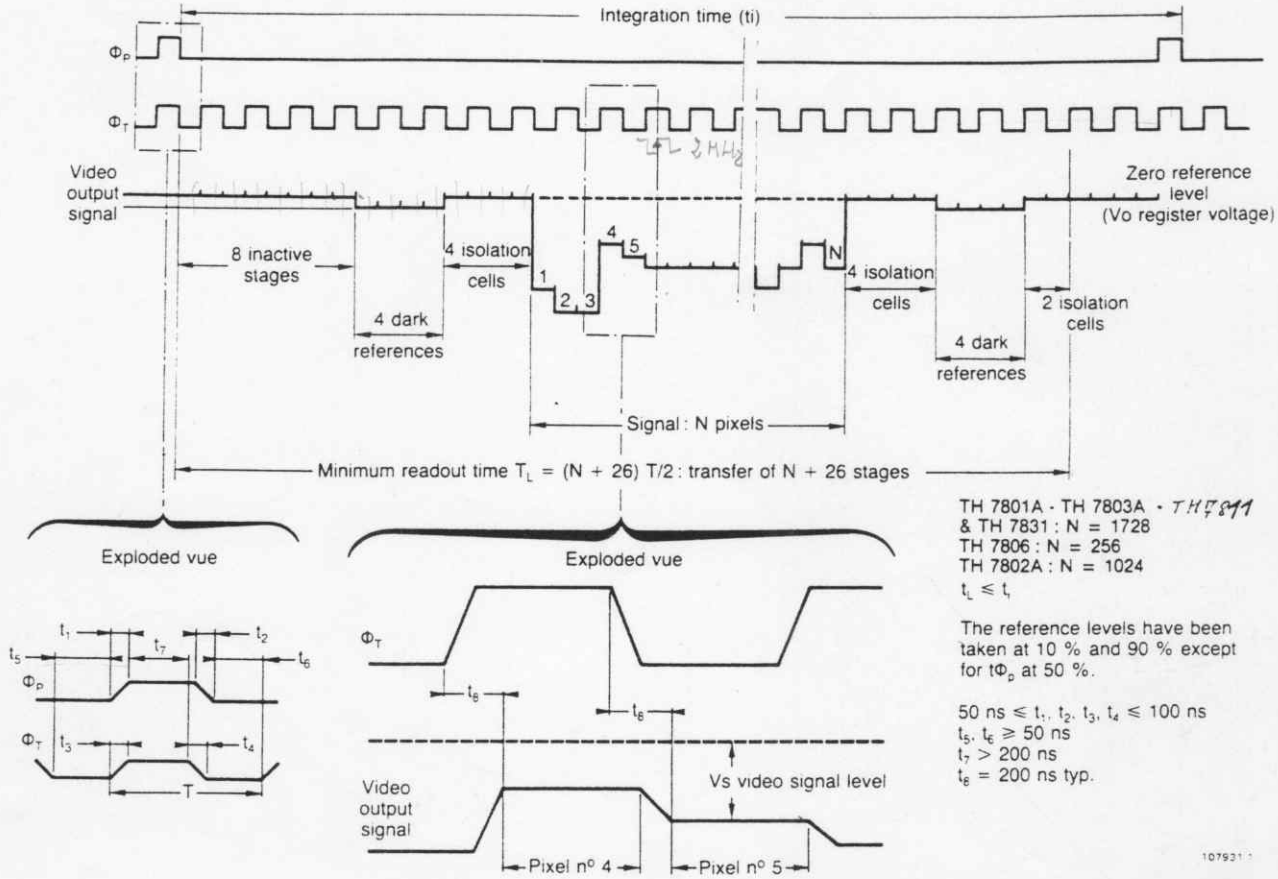


Figure 1 - Timing diagram of linear CCD drive signals

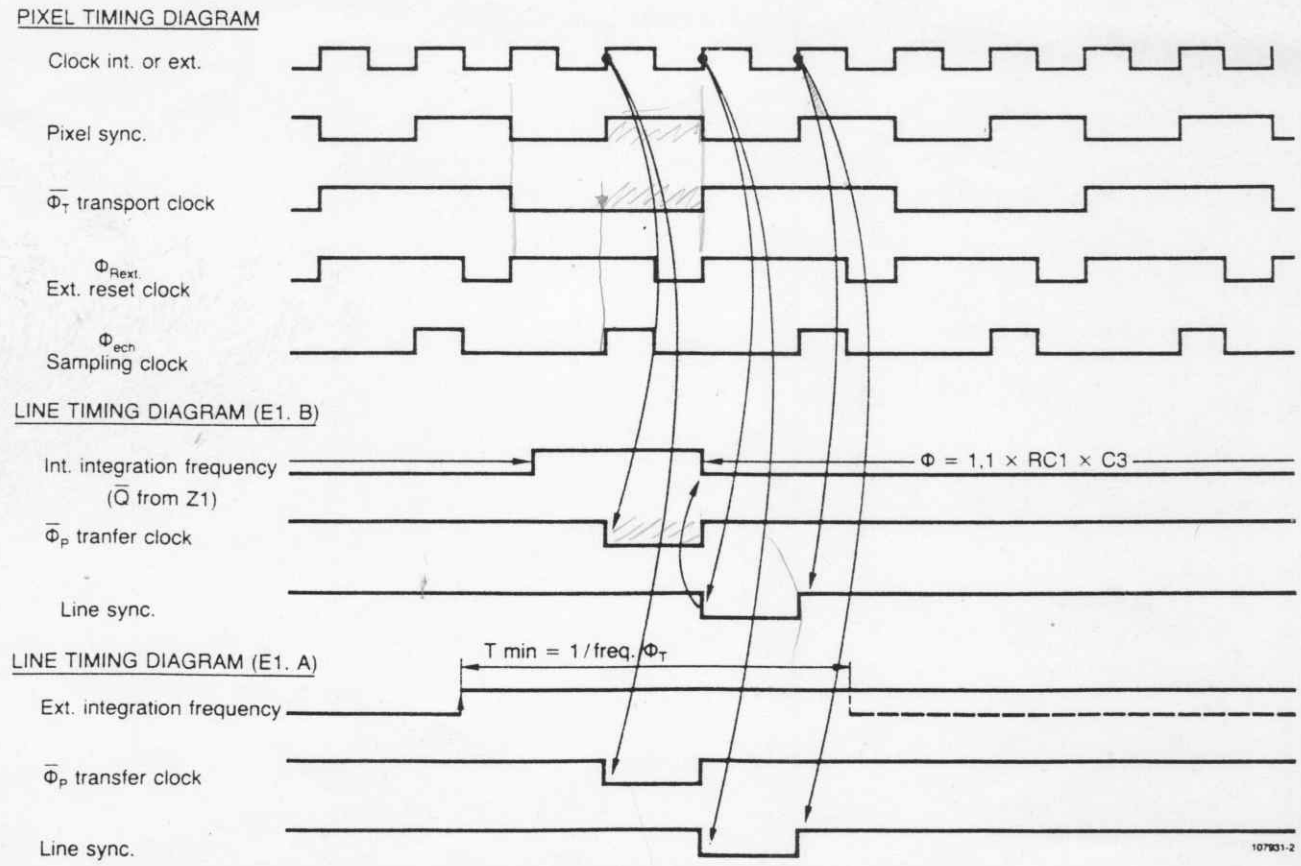
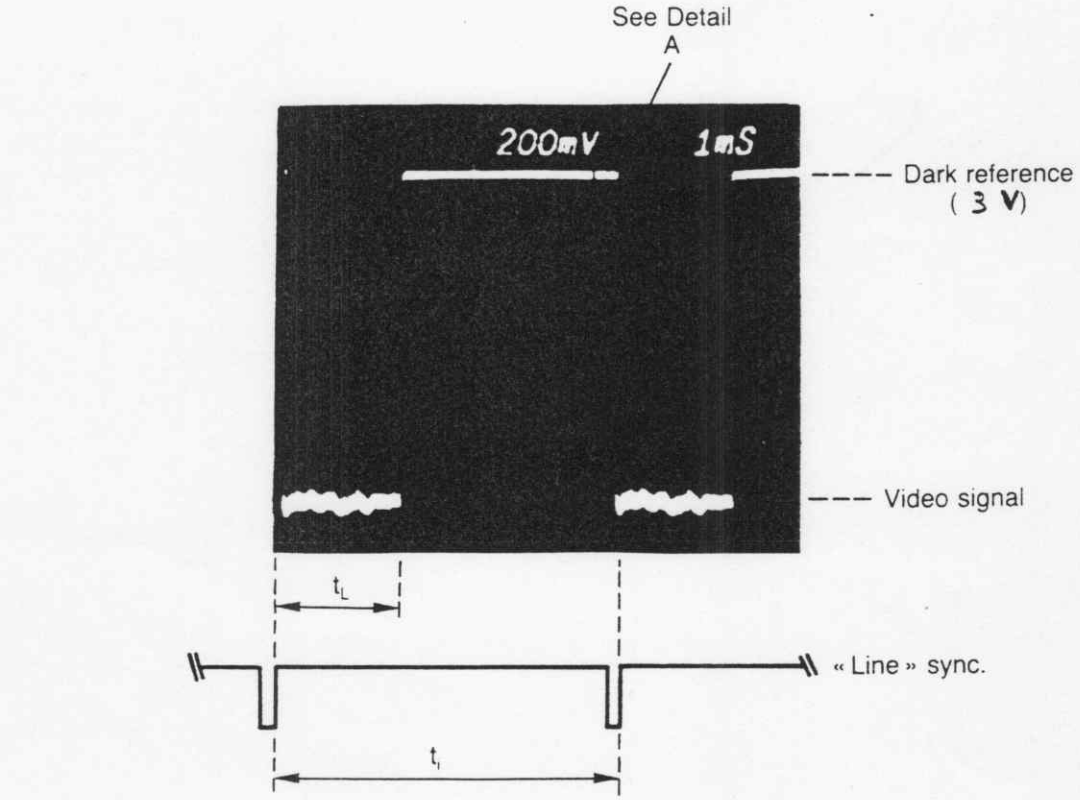


Figure 2 - Timing diagram of logic circuit command signals



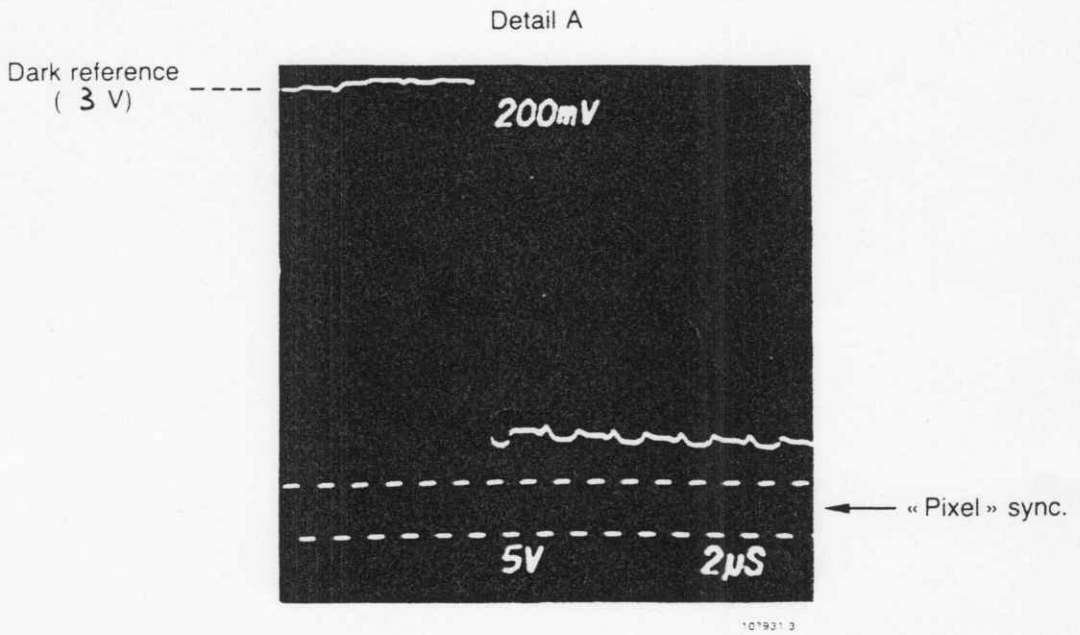


Figure 3 - Video output signal

ADJUSTMENTS

Integration Time

For nominal value of C_{11} = 220 nF :
The integration time (t_i) is adjustable from 3.5 ms to 25 ms by potentiometer RC3 ok

This adjustment range can be altered by replacing capacitor C_{11} with another capacitor C_x, the new integration times being given by the formula :

$$t_i = 1.1\ (R_{14} + R_{C3})\ C_x$$

where : t_i is in ms
RC3 in kΩ ; R_{14} = 15 kΩ
C_x is in µF.

Readout Time (ϕ_T)

For nominal C_{21} = 470 pF
The readout frequency (f_L) is adjustable between 500 kHz and 1.9 MHz by RC4 ok

The readout time (t_L) in ms is the number of CCD shift register stages divided by the readout frequency in kHz.

	TH 7801A TH 7803A TH 7831	TH 7802A	TH 7806 TH 7806(Z)
	(1754 stages)	(1050 stages)	(282 stages)
t_L min.	0.92 ms	0.55 ms	0.15 ms
t_L max.	3.5 ms	2.1 ms	0.56 ms

The above readout times (min. and max.) may be modified by replacing capacitor C_{21} by a capacitor C_y, the new readout times being given by the formula :

TH 7801A, TH 7803A, TH 7831

$$t_L\ max. = \frac{1754 \times C_y}{235} \cdot 10^{-3}$$

$$t_L\ min. = \frac{1754 \times C_y}{930} \cdot 10^{-3}$$

TH 7802A

$$t_L\ max. = \frac{1050 \times C_y}{235} \cdot 10^{-3}$$

$$t_L\ min. = \frac{1050 \times C_y}{930} \cdot 10^{-3}$$

TH 7806, TH 7806(Z)

$$t_L\ max. = \frac{282 \times C_y}{235} \cdot 10^{-3}$$

$$t_L\ min. = \frac{282 \times C_y}{930} \cdot 10^{-3}$$

C_y in pF ; t_L in ms.

Remark : If the original values for C_{21} and C_{11} have been changed, ensure that the readout time always remains shorter than the integration time.

Thus, at maximum readout frequency f_L = 1.9 MHz, the minimum integration time is 0.92 ms for the TH 7801A, TH 7803A, TH 7831 ; 0.55 ms for the TH 7802A and 0.15 ms for the TH 7806, TH 7806(Z).

Mean dc Output Level

The mean dc output level of the CCD varies according to the sensor (7 to 11 V typ.). The dc level on the inverting input of amplifier Z 1 may be adjusted using RG1 so as to obtain an amplifier output voltage of 6 V, i.e. 3 V on the video output with a load $Z_L = 50\ \Omega$.

Configurations

Several operating configurations are possible (see tables 3 & 4 and figure 5).

NB : The TH 7931 D is delivered with the following jumper configuration :

— ~~E1B~~ (E8A) E8B ..... integration time controlled by the board.
— ~~E2B and E3B~~ E7B and E6B ..... clock generated by the board.
— E3A and ~~E4B~~ E4A ..... use of internal reset clock.
— ~~E5B~~ E2B ..... internal sampling
— ~~E5A~~ E5A ..... without addition of pixels.
— ~~E8B~~ E1B ..... filtered and 50 Ω matched video output.

TYPICAL BIAS VALUES

The TH 7931D delivers all the necessary dc levels :
$V_{DD} = V_H = 14\ V$; $V_T = V_{GS} = V_{TP1} = 6.4\ V$ $V_{ST} = 6.4\ V$ These voltages ensure optimum operation irrespective of the sensor used and no adjustment of these values is necessary (especially for V_{TP} and V_{ST} whose values are not critical ; V_{ST} = + 5 to +7V, V_{TP} = + 5 to + 15V tolerated).

Bias values are indicated in the analog diagram, (figure 7)

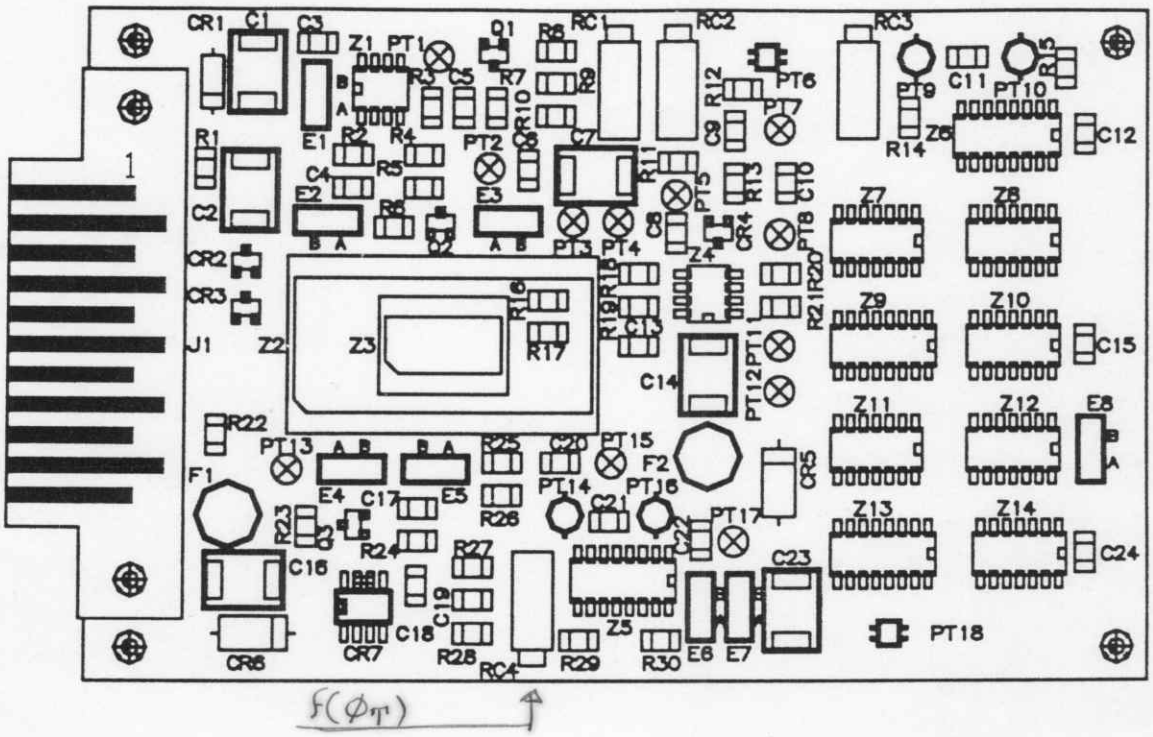
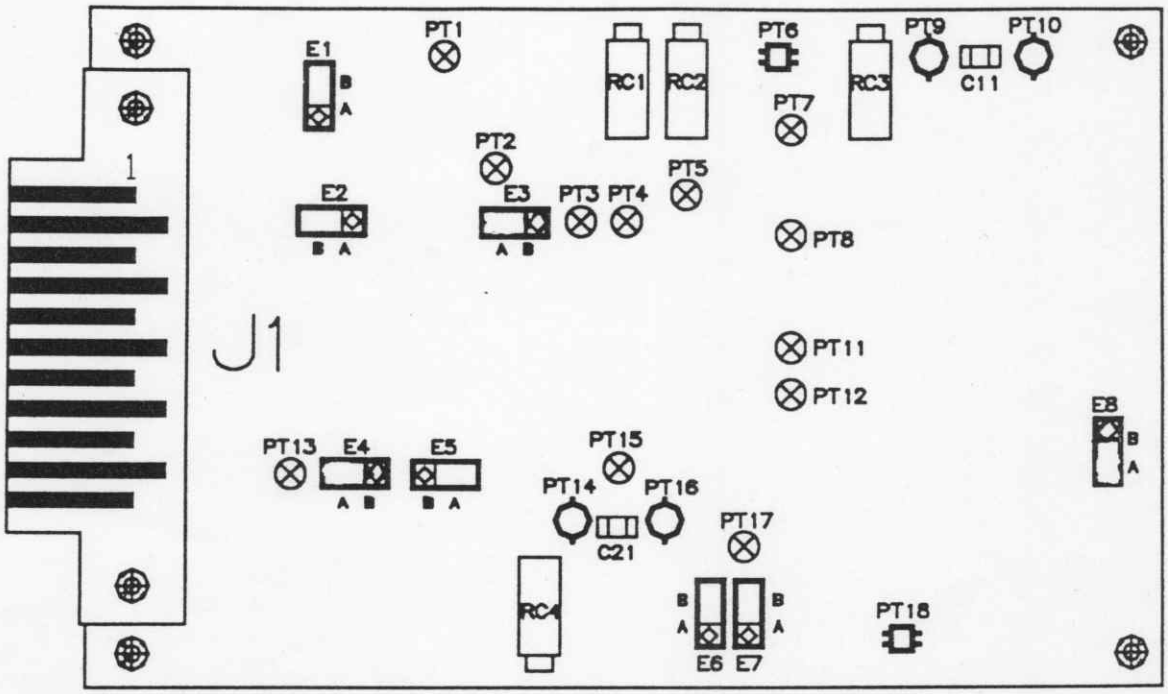


Figure 4 - Fitted printed circuit board



Note : Jumpers set for all internal operating mode
(exept for TH7831)

RC1	VA706 Biasing	RC3	Integration frequency
RC2	Antiblooming adjust	RC4	Pixel frequency

Figure 5 - Jumpers and variable resistors locations

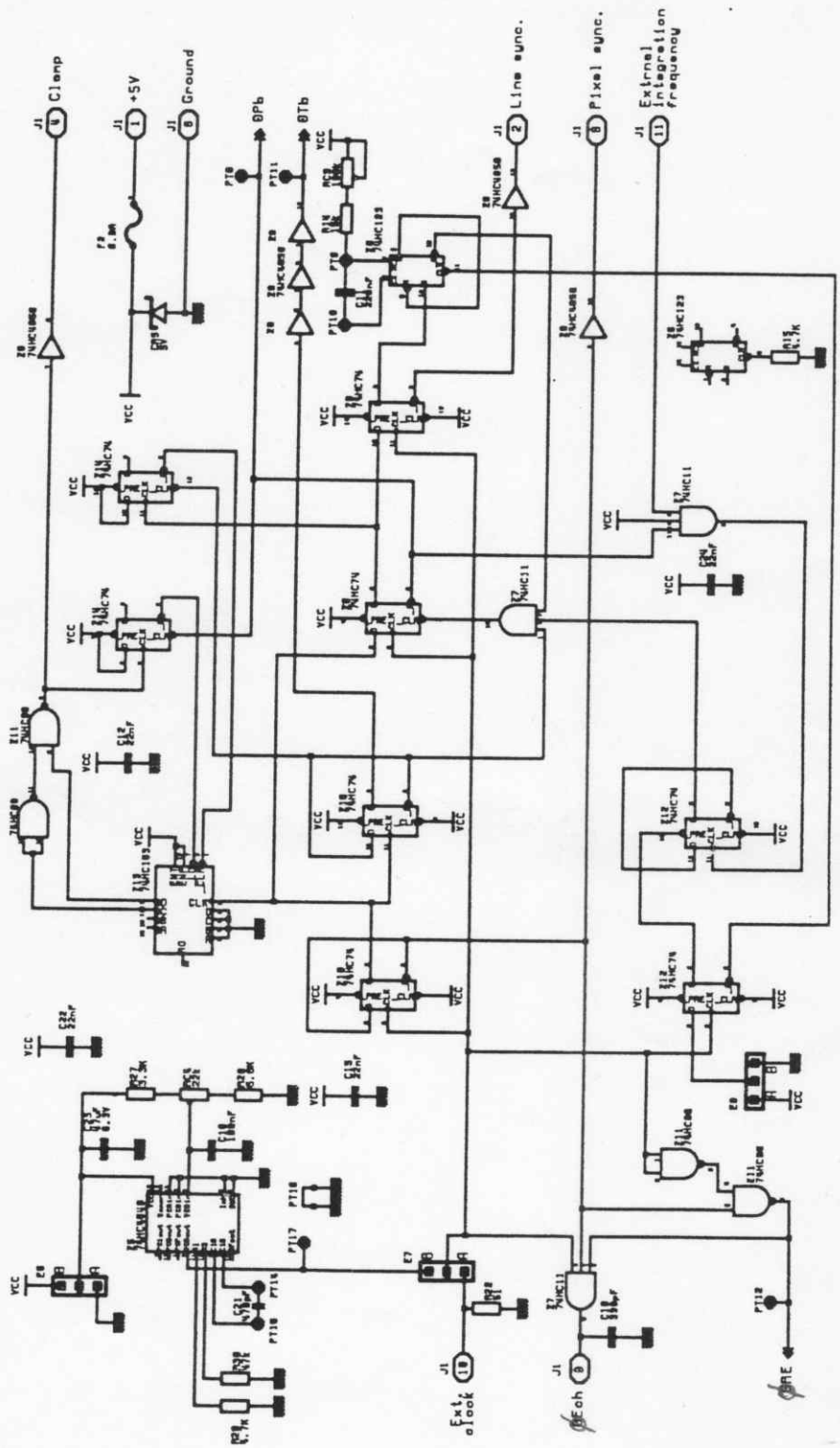


Figure 6 - Logic circuit diagramm

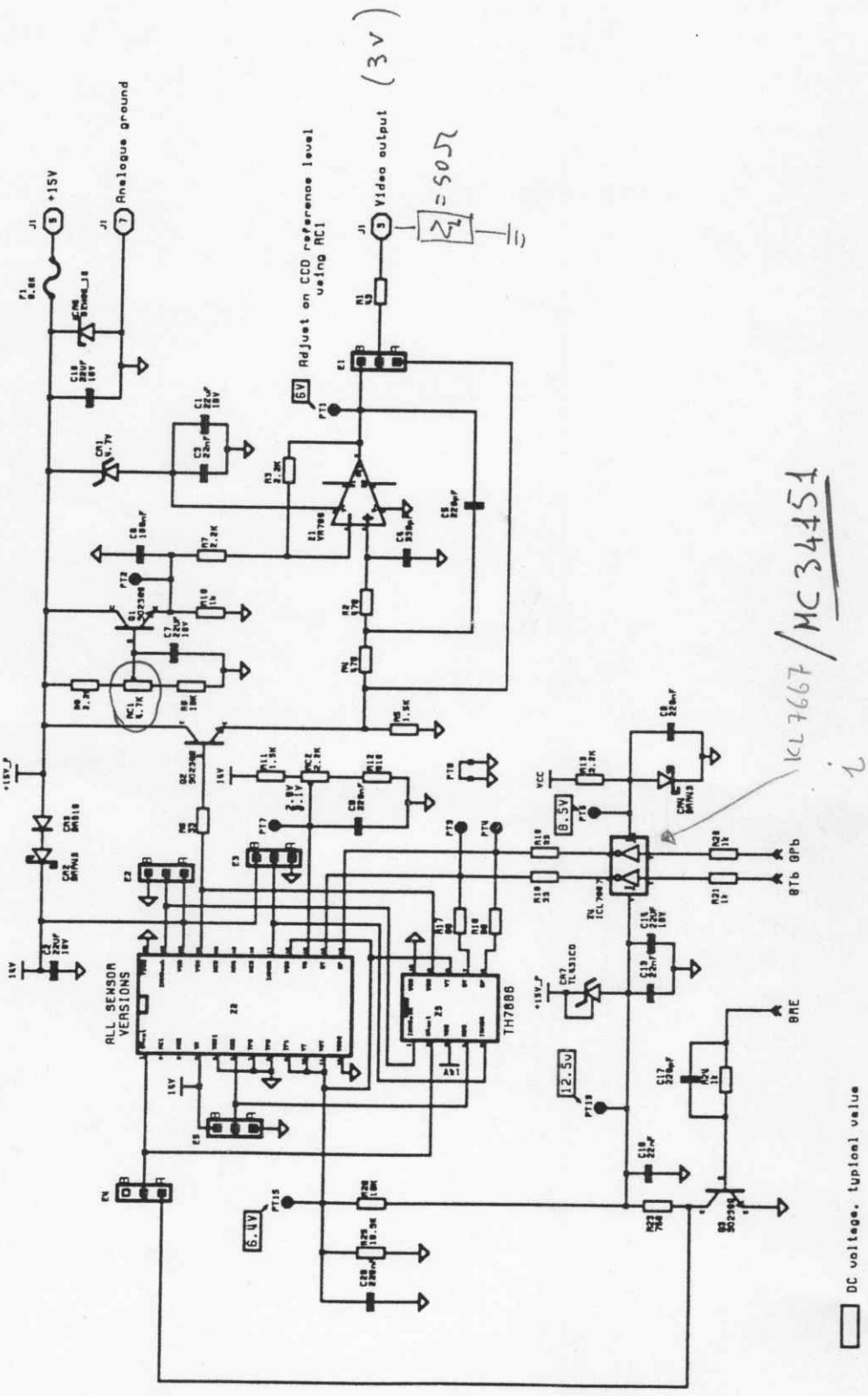


Figure 7 - Analog circuit diagramm

NT : Fonctions Not Tested
NC : Pin Not Connected
NU : Pin Not Used

		Linear CCD model						Drive module
		TH 7801A	TH 7802A	TH 7803A	TH 7806 TH 7806(Z)	TH 7811	TH 7831	TH 7931D
Number of photodiodes		1728	1024	1728	256	1728	1728	
Photodiodes size		13µm x13µm 13µm pitch	13µm x 13µm 13µm pitch	10µm x 13µm 10µm pitch	13µm x 13µm 13µm pitch	13µm x 13µm 13µm pitch	13µm x 39µm 13µm pitch	
Dark Reference position		8 inactive stages after ΦP and 4 dark reference stages at pixel frequency [2 . F ΦT]						
Max. Pixel Frequeny { MHz }		2	2	2	2	2	2	0.5 to 1.9
Integration Time on board { ms }		According to TH7931 D drive module setting						3.5 to 25
V_{DD} (pin 22) { volts }		14 ± 0.5	14 ± 0.5	13 ± 1.5	13 ± 1.5 (pin 3)	14 ± 0.5	14 ± 1.5	14
V_{SS} (pin 5-12-24) { volts }		0	0	0	0 (pin 10)	0	0 (pin 5= NU)	0
V_T (pin 10) Readout register bias { volts } **		6.4 ± 0.4	6.4 ± 0.4	6.7 ± 0.7	6.7 ± 0.7 (pin 8)	6.4 ± 0.4	6.4 ± 0.4	6.4
V_{ST} (pin 11) Photosensitive zone bias { volts }		Min Typ Max 5.5 V_T 7	Min Typ Max 5.5 V_T 7	Min Typ Max V_T - 7.4	no external connection	Min Typ Max 5.5 V_T 7	Min Typ Max 5.5 V_T 7	6.4
V_{GS} [may be connected to V_T] (pin 16) Output Gate { volts }		V_T	V_T	V_T	no external connection	V_T	V_T	6.4
V_H (pin 4) Internal Logic supply { volts }		V_{DD}	V_{DD}	V_{DD}	no external connection	V_{DD}	V_{DD}	14
TP1 [may be connected to V_{ST}] (pin9) Test point 1 { volts }		V_{DD}	V_{DD}	V_{DD}	no external connection	V_{DD}	V_{DD}	14
TP2 and TP3 (pins 8 and 7) Test points 2 and 3 { volts }		V_{SS}	V_{SS}	V_{SS}	no external connection	V_{SS}	V_{SS}	0
ΦT [ampl.] (pin 14) Transfert clocks { volts }	High	12.5 ± 0.5	12.5 ± 0.5	13 ± 1.5	13 ± 1.5 ΦT (pin 7)	12.5 ± 0.5	12.5 ± 0.5	12.5
ΦP [ampl.] (pin 13) Transfert clocks { volts }					ΦP (pin 6)			
ΦR [ampl.] (pin 1) Reset clocks { volts }	Low	0.3 ± 0.3	0.3 ± 0.3	0.3 ± 0.3	0.3 ± 0.3 ΦR (pin 2)	0.3 ± 0.3	0.3 ± 0.3	0.5
ΦR Inhibit (pin 17) Input pin with Pull Up	Off	NC or V_{DD}	NC or V_{DD}	NC or V_{DD}	NC or V_{DD} NT (pin 5)	NC or V_{DD}	NU (No Internal Reset Clock)	V_{DD}
	On	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{SS}
Inhibit Φ_{ech} (pin 23) Input pin with Pull Down	Off	NC or V_{SS}	NC or V_{SS}	NC or V_{SS}	NC or V_{SS} NT (pin 1)	NC or V_{SS}	NC or V_{SS}	V_{SS}
	On	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
ADD [pixel addition] (pin 6) Input pin with Pull Down	Off	NC or V_{SS}	NC or V_{SS}	NC or V_{SS}	NC or V_{SS} NT (pin 4)	NC or V_{SS}	NC	V_{SS}
	On	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}		V_{DD}
Pins 2-3-15-18-19-20		NU	NU	NU	No Pins	NU (pin 15= V_A) *	NU	NU
Video output : pin 21, except TH7806 : pin 9								

* : V_A = Antiblooming control {DC Bias 3 to 9 volts } for TH7811 pin 15 [without AB : V_A = 3 volts]

** : $V_T = [(\Phi T_{High\ Level} + \Phi T_{Low\ Level}) + 2] \pm 5\%$

TABLE 1 - Linear CCD and drive module signal levels

Table 2 - Pin-out of TH 7931D connector

Pin no.	Designation
1	+ 5 V
2	Line sync. output
3	50 Ω matched video output
4	Clamp pulse output
5	+ 15 V
6	Logic ground (+5 gnd)
7	Analog ground (+15 gnd)
8	Pixel sync. output
9	Sampling clock output
10	Readout time command input (or ext. clock)
11	Integration time command input (or ext. integration frequency)

Table 3 - TH 7931D operating modes

Function modified	Configuration		Jumper
	Jumper in position A	Jumper in position B	
Integration frequency	External	Internal OK	E8
Clock	External	Internal	E7 and E6
Φ reset	External	Internal	E3 and E4
Inhibit sampling Φ on TH 7801A TH 7802A TH 7803A TH 7806 TH 7806(Z) TH 7831	without sampling	Normal mode internally sampled video output	E2
Pixel pairing	No	Yes	E5
50 Ω matched video signal	Unfiltered	Filtered	E1

Table 4 - Jumper selections for different operating modes

Operating mode	E8	E6 E7	E3 E4	E2	E5	E6 E1
All internal	A or B	A or B	A	B	A	A or B
Internal sampling and external Φ_R [CCD TH 7831]	A or B	A or B	B	B	A	A or B
Unsampled video output internal Φ_R	A or B	A or B	A	A	A	A or B
Unsampled video output external Φ_R	A or B	A or B	B	A	A	A or B
Pixel pairing	A or B	A or B	A	B	B	A or B